EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Ultralow-cost, two-digit counter features few components

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

The ultralow-cost, two-digit-counter circuit in Figure 1 represents an attempt to reduce the number of components using a mostly software approach and a low-cost microcontroller, the PIC16F84A. The circuit lacks the current-limiting resistors that normally connect to a seven-segment LED display's pins because a software routine lights only one of the display's segments at a time, first in the 10s display and then in the units display. Doing so keeps the circuit's maximum current consumption at a nearly constant level, even if you add a third LED display to implement a three-digit counter. The circuit also lacks digit-selection switching transistors that classic multiplexed circuits' switching transistors typically use, and the circuit includes one common-cathode and one common-anode display. The reason for this approach is that each of the microprocessor's I/O Port A and Port B lines can assume one of three states: high, low, and floating—that is, high impedance. Programming a line as an input places it in a high-impedance state, which turns the display off.

In addition, the program drives only one segment at a time and executes the following sequence: To drive the 10s display, program the line RB0 output and drive it high to light the corresponding segment of the common-cathode display and then program RB0 as an input. Repeat this procedure for lines RB1 through RB6. To drive the units display, repeat the process while applying a low output from RB0 to drive the common-anode display. Figure 2 shows the circuit's timing diagram. The prototype display uses Kingbright's (www.kingbright.com) SC52-11EWA (DS_1) and SA52-11EWA (DS_2) high-efficiency, seven-segment displays that emit 2000 to 5600 µcd at a forward current of 10 mA. At a forward current of approximately 5 mA, the displays remain readable.

Early motion pictures displayed at an 18-Hz rate, which produces marginal flicker. The software executes at a rate of 180 Hz, or 10 times the minimum flicker rate. Each of the display's seven segments must illuminate for an interval of 1/(180×7) sec, or approximately 0.8 msec. To simplify the timing routine (section Delay3 of Listing 1, available at www.edn.com/060817di1), the software uses a refresh interval of 1 msec.

Although this approach provides adequate segment-drive current, the display's internal LEDs carry a 3V maximum reverse-voltage rating. Driving any I/O line high applies forward bias to one segment of the common-cathode digit but applies reverse bias to the

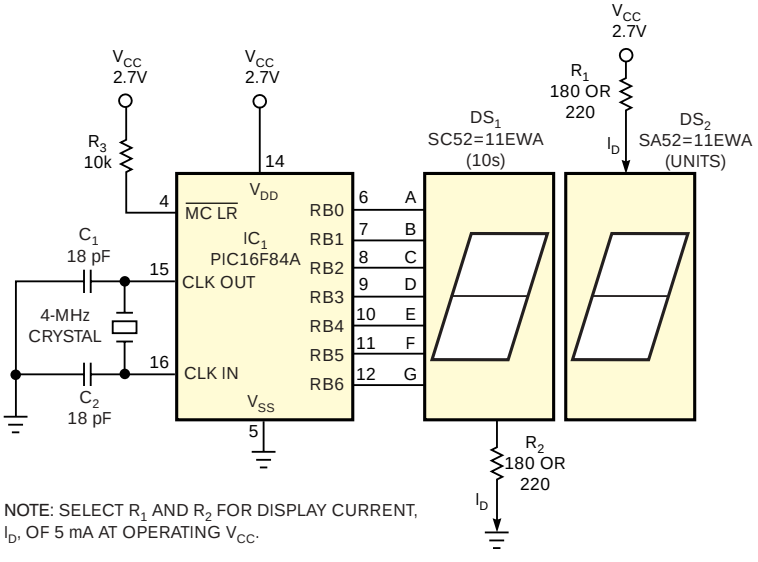

Figure 1 This low-cost, two-digit counter uses few components.

DIs Inside

70 Two-wire, four-by-four-key keyboard interface saves power

74 Gain-of-three amplifier requires no external resistors

▶What are your design problems and solutions? Publish them here and receive $150! Send your Design Ideas to edndesignideas@reedbusiness.com.

corresponding segment of the common-anode display. The 16F84A requires a minimum of 2V for operation, and thus the circuit must operate in a 2 to 3V power-supply range. The assembler source code in Listing 1 counts from 0 to 99 sec and serves as an unoptimized proof-of-concept software test bed for the display. EDN

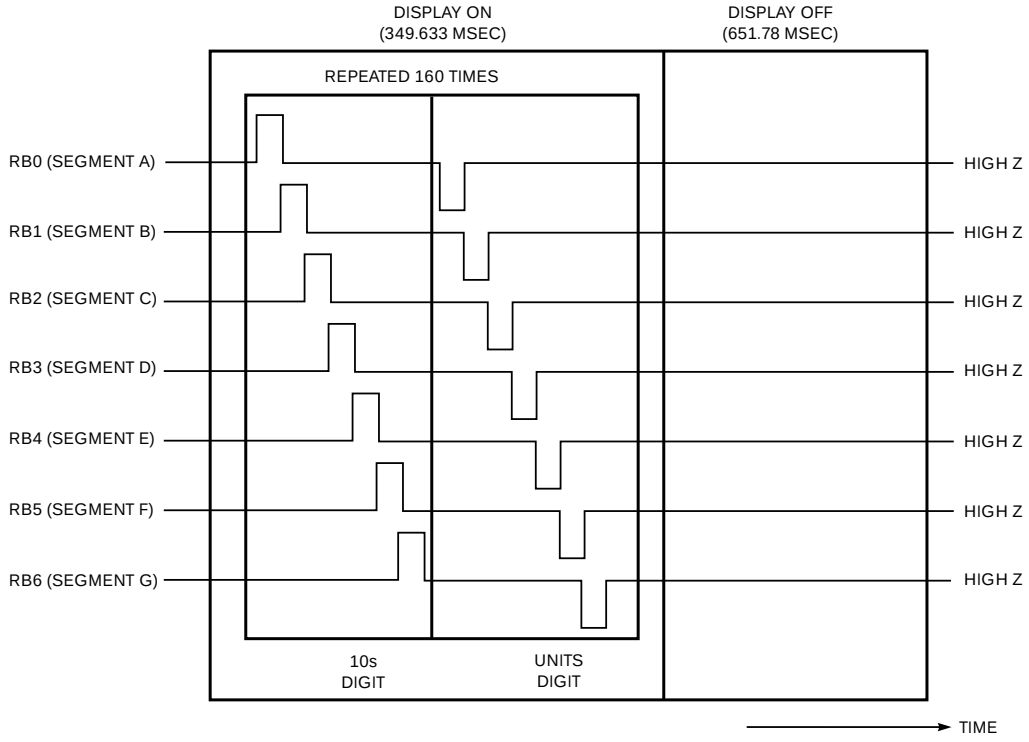

Figure 2 The timing diagram illustrates segment- and digit-drive intervals.

Two-wire, four-by-four-key keyboard interface saves power

Stefano Salvatori, University of Rome, Rome, Italy,
and Gabriele Di Nucci, EngSistemi, Rome, Italy

You can use a microcontroller that includes an ADC to design a two-wire-plus-ground keyboard interface. For example, you can use a resistive voltage divider to identify a pressed key (Reference 1). A microcontroller's integrated ADC typically presents an input resistance on the order of hundreds of kilohms, and, for adequate accuracy, its keypad divider should comprise relatively low-value resistors of 10s of kilohms. However, in battery-powered systems, a resistive divider can consume a few hundred microamperes, forcing a designer to choose an alternative classic digital-matrix array of switches and multiple I/O lines. Moreover, portable-equipment designs typically place constraints on the number of components.

To satisfy both requirements, the circuit in Figure 1 uses a matrix keypad and a resistor network divided into two row and column sections. For the four-by-four-key keypad, seven resistors are sufficient to encode any pressed key, and the circuit consumes power only while a key remains closed. Conversely, with no keys pressed, the standby current approaches zero. Using only two values of resistors, let $R_A=R_B=R_C=R_1$ and $R_D=R_E=R_F=R_G=R_2$. Assigning values from zero to three for the keys' x and y addresses, you can calculate the voltage across resistor R_G for any key closure by solving the following equation:

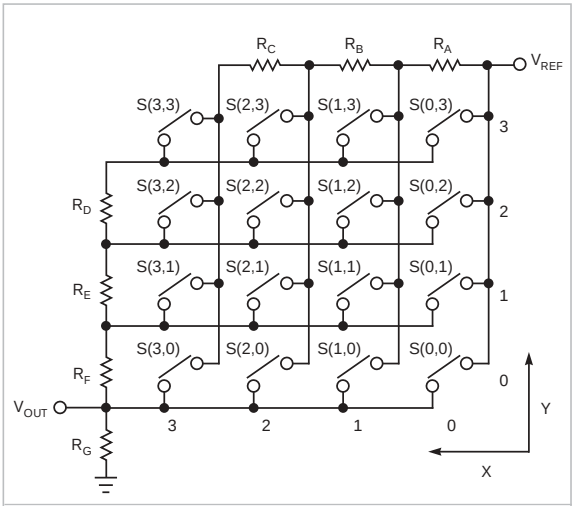

Figure 1 A two-wire resistive voltage-divider interface encodes a four-row-by-four-column keypad.

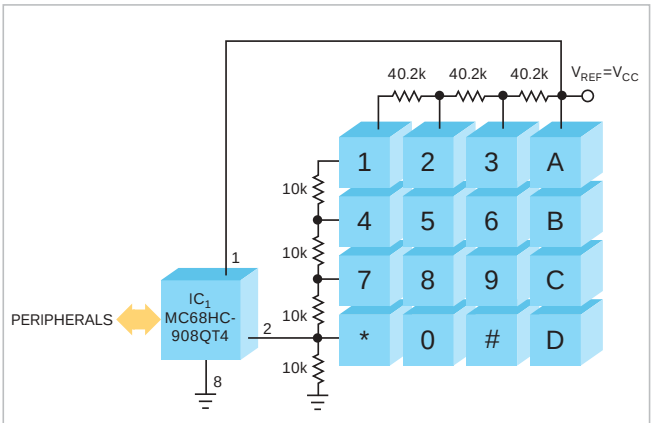

Figure 2 Using the microcontroller's analog reference-voltage output and ratiometric analog-to-digital conversion ensures correct encoding of the keypad.

TABLE 1 SINGLE-KEY OUTPUT CODES

Keys pressed/resistance (Ω)

Y \ X	3	2	1	0
3	1/ 15 to 16	2/ 21	3/ 32	A/ 63 to 64
2	4/ 17	5/ 23	6/ 36	B/ 85
1	7/ 18	8/ 25	9/ 42	C/ 127
0	*/ 19	8/ 28	#/ 51	D/ 255

Note: The figures preceding the slashes represent the keypad's key labels.

TABLE 2 TWO-KEY OUTPUT CODES

Keys pressed	Resistance (Ω)
C+#	141 to 142
C+0	134 to 135
C+*	132
B+#	109
B+0	98
B+9	91
B+8	88
A+8	76
A+7	70 to 71
A+6	68

$$V(x,y)=V_{REF}\times\frac{R_2}{x\times R_1+y\times R_2+R_2}.$$

Driving the resistor array from V_{REF}, the ADC's reference voltage, allows you to perform a ratiometric conversion that eliminates errors in key encoding due to fluctuations in V_{REF}. The following equation describes the voltage-division ratio, r(x,y), for any keystroke.

$$r(x,y)=\frac{V(x,y)}{V_{REF}}=\frac{1}{(1+x\times p+y)}.$$

The ratio $p=R_1/R_2$ represents the ratio between row- and column-group resistors' values. For p=4, you calculate 16 values of r(x,y), in the [1/16, 1] range, as a function of the pressed key's position. In general, the minimum difference between r partitioning ratios occurs for the nearest keys as the (3,2) and (3,3) x,y indexes indicate. For an N-bit ADC and a ratio of p=4, the ADC should have a resolution that satisfies the following equation: $2^{-N}<r(3,2)-r(3,3)=15^{-1}-16^{-1}=240^{-1}$. Note that the reciprocal of 240 (0.0041...) exceeds the reciprocal of 2^8, and the circuit thus requires an ADC capable of at least 8-bit resolution ($N\geq 8$ bits).

Unfortunately, standard-value components with nominal tolerance, T, cannot provide an ideal solution to this equation. Instead, you calculate a partitioning-ratio difference, $d=r(3,2)-r(3,3)$, for the worst-case condition. The lowest value of d occurs for a minimum value of R_G and R_D and the maximum value of R_A, R_B, R_C, R_E, and R_F. You can account for all the resistors' values and define a generic ratio, p, for the nominal values of R_1 and R_2:

$$d_{MIN}(p,T)=(1-T)^2/\{[3\times(p+1)+(3p+1)\times T]\times[(3p+4)+3\times p\times T]\}>2^{-N}.$$

The same value of T applies to all resistors. If n=8 and p=4, the previous equation yields a solution of T<0.018, which indicates that resistors of ±1% tolerance correctly encode 16 keys. Moreover, if you now impose the chosen fixed tolerance, T, you can solve the equation to obtain the required limit on the p ratio between the values of R_1 and R_2. If T=0.01, the solution to the equation becomes p<4.074.

The circuit in Figure 2 uses Freescale's (www.freescale.com) Nitron MC68HC-908QT4 microprocessor, which serves as a test bed for a keypad based on the above-calculated values, and uses pow-

er-supply voltage V_{CC} as the resistor matrix's reference voltage, V_{REF}. To satisfy the requirement for p(4.074 >p>4), use R_1=10 kΩ±1% tolerance and R_2=40.2 kΩ±1% tolerance, both standard values that the E48 series offers. Table 1 lists output codes corresponding to 16 individually pressed keys, and Table 2 lists data obtained when simultaneously pressing two keys and illustrates that two-key combinations can evoke special functions.

If your application requires a microcontroller that lacks an internal interrupt that the ADC generates, you can connect an external comparator to the output voltage in Figure 1. Set the comparator's threshold lower than the lowest voltage developed at the output voltage—approximately V_{REF} divided by 16 in the example—and the comparator's output serves as a keypad-interrupt source for the microcontroller.

Note that a microcontroller with a 10-bit ADC, such as a Freescale MC68HC908QB or a Texas Instruments (www.ti.com) MSP430F11 can service a five-row by six-column keypad matrix encoded by 10 resistors. Repeating the analysis shows that a row-to-column p ratio of 5 to 5.51 and a required resistor tolerance of less than 4.3% correctly encode the keys. You can use values of 10 kΩ for R_1 and 51.1 kΩ or 53.6 kΩ for R_2 of the ±1%-tolerance E48 series.

REFERENCE

1. Amorim, Vitor, and J Simões, "ADC circuit optimizes key encoding," *EDN*, Feb 4, 1999, pg 101, www.edn.com/article/CA56657.

Gain-of-three amplifier requires no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Analog Devices' ADA4862-3 comprises three wideband amplifiers, each configured by an internal, fixed-value resistive-feedback network as a noninverting gain-of-two amplifier. Due to its internal feedback networks, the device offers a bandwidth of 300 MHz and excellent insensitivity to stray capacitance, variations in pc-board layout, and proximity of other devices. According to its specifications, each of IC_1's three internal amplifiers offers

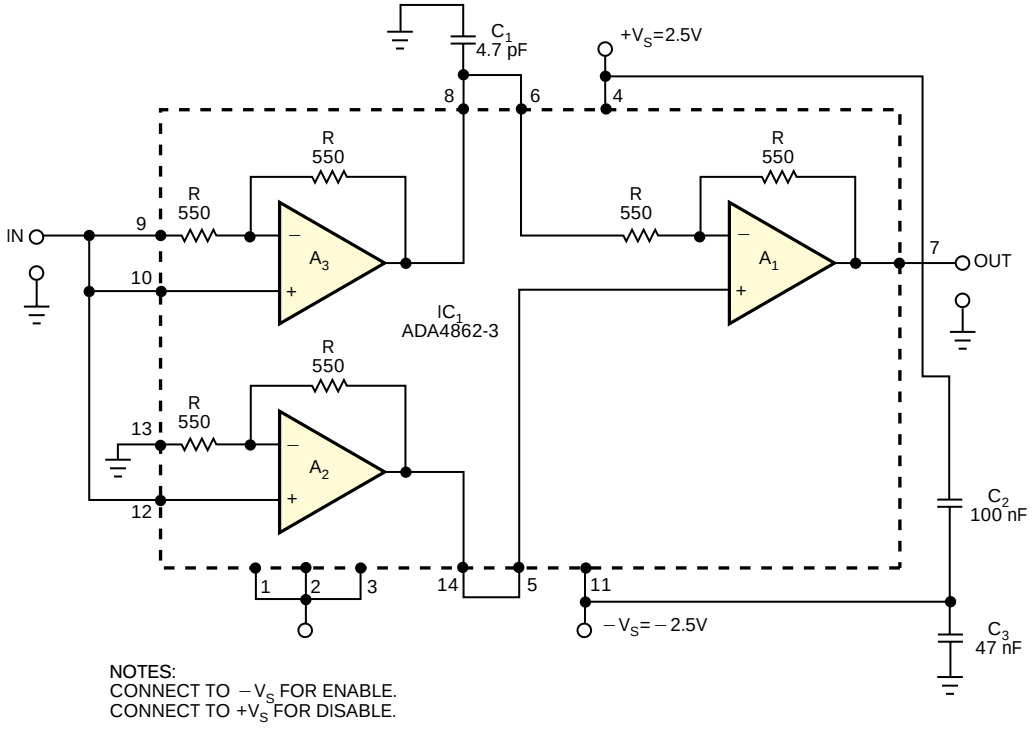

Figure 1 A one-IC amplifier with a voltage gain of three provides flat response to more than 60 MHz.

three gain configurations—two, one, or negative one (Reference 1). When you configure it for a gain of two, a cascade of two or three amplifiers yields gains of four or eight, respectively. If your application requires a gain of three, you can use the circuit in Figure 1. Amplifier A_3 serves as an impedance converter with a net voltage gain of one and a low-impedance driver for A_1's gain-setting network. Amplifier A_2 provides a gain of two at its noninverting input.

In addition, A_3 introduces the proper time delay (phase shift) in A_1's inverting-input path and thus roughly equalizes the time delay in A_1's noninverting signal path. This configuration improves the circuit's dynamic performance over that you can achieve when A_1's inverting input connects directly to the input signal. A 4.7-pF chip capacitor that connects from voltage follower A_3's output to ground reduces the voltage follower's output impedance at frequencies of 100 MHz and above to ensure A_1's stability.

MORE AT EDN.COM

For more Design Ideas, visit www.edn.com/designideas.

For our best entries, go to www.edn.com/bestofdesignideas.

If you configure it as a differential amplifier, A_1 amplifies the input signal by a factor of two at its noninverting input and by a factor of negative one at its inverting input. The final voltage at A_1's output comprises the algebraic sum of both components: $V_{OUT}=4\times V_{IN}-V_{IN}=3\times V_{IN}$. In a conventional voltage amplifier, reducing negative feedback increases the overall gain. In contrast, cascading amplifiers with negative-voltage-feedback networks only slightly reduces the circuit's bandwidth. The net gain decrease at a frequency of 65 MHz amounts to 0.1 dB, or approximately 1.15% of a single gain-of-two amplifier's dc gain. For the gain-of-three amplifier in Figure 1, the gain decrease at 65 MHz amounts to approximately 2.3% of the circuit's dc gain.

For the best high-frequency performance, connect the ADA4862's internal amplifiers as Figure 1 shows to minimize the lengths of the device's external interconnections. You can cascade additional ADA4862-3 ICs to produce any gain expressed as $3^M\times 2^N$, where M and N represent integers, including zero—that is, gains of six, nine, 12, and so on. EDN

REFERENCE

1. ADA4862-3 data sheet, Analog Devices Inc, www.analog.com/UploadedFiles/Data_Sheets/360747397ADA4862_3_a.pdf.